

NBXDBA015, NBXDDB015

3.3 V, 200.0 MHz/206.9 MHz Dual Frequency LVPECL Clock Oscillator

The NBXDBA015/NBXDDB015 dual frequency crystal oscillator (XO) is designed to meet today's requirements for 3.3 V LVPECL clock generation applications. The device uses a high Q fundamental crystal and Phase Lock Loop (PLL) multiplier to provide selectable 200.0 MHz or 206.9 MHz, ultra low jitter and phase noise LVPECL differential output.

This device is a member of ON Semiconductor's PureEdge™ clock family that provides accurate and precision clock solutions.

Available in 5 mm x 7 mm SMD (CLCC) package on 16 mm tape and reel in quantities of 1,000. Frequency stability options available as either 50 PPM NBXDBA015 or 20 PPM NBXDDB015*.

Features

- LVPECL Differential Output
- Uses High Q Fundamental Mode Crystal and PLL Multiplier
- Ultra Low Jitter and Phase Noise – 0.4 ps (12 kHz – 20 MHz)
- Selectable Output Frequency – 200.0 MHz (default)/206.9 MHz
- Hermetically Sealed Ceramic SMD Package
- RoHS Compliant
- Operating Range 3.3 V $\pm 10\%$
- Total Frequency Stability – ± 20 PPM* or ± 50 PPM

Applications

- High-End Servers
- Basestations
- General Purpose Clock Generation and Margining

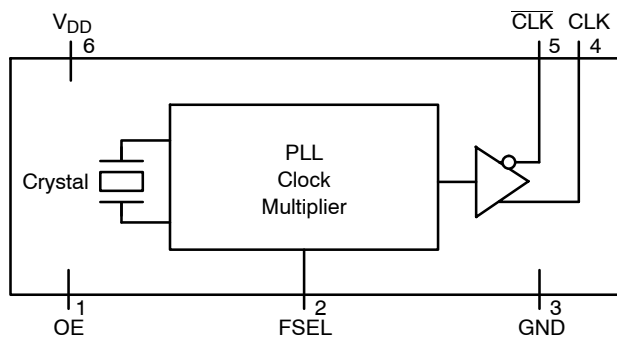
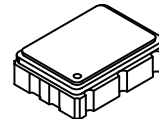


Figure 1. Simplified Logic Diagram



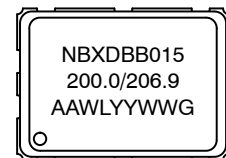
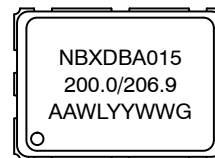
ON Semiconductor®

<http://onsemi.com>



6 PIN CLCC
LN SUFFIX
CASE 848AB

MARKING DIAGRAMS



NBXDBA015 = NBXDBA015 (± 50 PPM)
 NBXDDB015 = NBXDDB015 (± 20 PPM)*
 200.0/206.9 = Output Frequency (MHz)
 AA = Assembly Location
 WL = Wafer Lot
 YY = Year
 WW = Work Week
 G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NBXDDB015LN1TAG*	CLCC-6 (Pb-Free)	1000/ Tape & Reel
NBXDBA015LN1TAG	CLCC-6 (Pb-Free)	1000/ Tape & Reel
NBXDBA015LNHTAG	CLCC-6 (Pb-Free)	100/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

* Please contact sales office for availability

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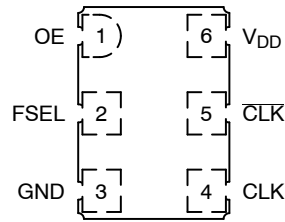


Figure 2. Pin Connections (Top View)

Table 1. PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	OE	LVTTTL/LVCMOS Control Input	Output Enable Pin. When left floating pin defaults to logic HIGH and output is active. See OE pin description Table 2.
2	FSEL	Control Input	Output Frequency Select Pin. Pin will default LOW when left open. See Output Frequency Select Table 3.
3	GND	Power Supply	Ground 0 V.
4	CLK	LVPECL Output	Non-Inverted Clock Output. Typically loaded with 50 Ω receiver termination resistor to $V_{TT} = V_{DD} - 2 V$.
5	$\overline{\text{CLK}}$	LVPECL Output	Inverted Clock Output. Typically loaded with 50 Ω receiver termination resistor to $V_{TT} = V_{DD} - 2 V$.
6	V_{DD}	Power Supply	Positive power supply voltage. Voltage should not exceed 3.3 V ±10%.

Table 2. OUTPUT ENABLE TRI-STATE FUNCTION

OE Pin	Output Pins
Open	Active
High Level	Active
Low Level	High Z

Table 3. OUTPUT FREQUENCY SELECT

FSEL Pin	Output Frequency (MHz)
Open (pin will float Low)	200
High Level	206.9
Low Level	200

Table 4. ATTRIBUTES

Characteristic	Value
Input Default State Resistor	170 kΩ
ESD Protection	Human Body Model Machine Model 2 kV 200 V
Meets or Exceeds JEDEC Standard EIA/JESD78 IC Latchup Test	

1. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

Table 5. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{DD}	Positive Power Supply	GND = 0 V		4.6	V
I_{out}	LVPECL Output Current	Continuous Surge		25 50	mA
T_A	Operating Temperature Range			-40 to +85	°C
T_{stg}	Storage Temperature Range			-55 to +120	°C
T_{sol}	Wave Solder	See Figure 6		260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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Table 6. DC CHARACTERISTICS ($V_{DD} = 3.3\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Symbol	Characteristic	Conditions	Min.	Typ.	Max.	Units
I_{DD}	Power Supply Current (Note 2)			82	100	mA
V_{IH}	OE Input HIGH Voltage		2000		V_{DD}	mV
V_{IL}	OE Input LOW Voltage		$GND - 300$		800	mV
I_{IH}	Input HIGH Current	OE	-100		+100	μA
		FSEL	-100		+100	
I_{IL}	Input LOW Current	OE	-100		+100	μA
		FSEL	-100		+100	
V_{IH}	FSEL Input HIGH Voltage		2000		V_{DD}	mV
V_{IL}	FSEL Input LOW Voltage		0		800	mV
V_{OH}	Output HIGH Voltage (Note 2)	$V_{DD} = 3.3\text{ V}$	$V_{DD}-1195$ 2105		$V_{DD}-945$ 2355	mV
V_{OL}	Output LOW Voltage (Note 2)	$V_{DD} = 3.3\text{ V}$	$V_{DD}-1945$ 1355		$V_{DD}-1600$ 1700	mV
V_{OUTPP}	Output Voltage Amplitude (Note 2)			700		mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Measurement taken with outputs terminated with 50 ohm to $V_{DD}-2\text{ V}$. See Figure 5.

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Table 7. AC CHARACTERISTICS ($V_{DD} = 3.3 \text{ V} \pm 10\%$, $GND = 0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$) (Note 3)

Symbol	Characteristic	Conditions	Min.	Typ.	Max.	Units
f_{CLKOUT}	Output Clock Frequency	FSEL = HIGH		206.9		MHz
		FSEL = LOW		200		
Δf	Frequency Stability – NBXDBB015* – NBXDBA015	0°C to $+70^\circ\text{C}$ -60°C to $+85^\circ\text{C}$ (Note 4)			$\pm 20^*$ ± 50	ppm
Φ_{NOISE}	Phase-Noise Performance $f_{\text{CLKout}} = 200 \text{ MHz}/206.9 \text{ MHz}$ (See Figures 3 and 4)	100 Hz of Carrier		-102		dBc/Hz
		1 kHz of Carrier		-119		dBc/Hz
		10 kHz of Carrier		-126		dBc/Hz
		100 kHz of Carrier		-127		dBc/Hz
		1 MHz of Carrier		-135		dBc/Hz
		10 MHz of Carrier		-160		dBc/Hz
$t_{\text{jitter}}(\Phi)$	RMS Phase Jitter	12 kHz to 20 MHz		0.4	0.9	ps
t_{jitter}	Cycle to Cycle, RMS	1000 Cycles		1.5	8	ps
	Cycle to Cycle, Peak-to-Peak	1000 Cycles		10	30	ps
	Period, RMS	10,000 Cycles		1	4	ps
	Period, Peak-to-Peak	10,000 Cycles		7	20	ps
$t_{\text{OE/OD}}$	Output Enable/Disable Time				200	ns
$t_{\text{DUTY_CYCLE}}$	Output Clock Duty Cycle (Measured at Cross Point)		48	50	52	%
t_{R}	Output Rise Time (20% and 80%)			250	400	ps
t_{F}	Output Fall Time (80% and 20%)			250	400	ps
t_{start}	Start-up Time			1	5	ms
		Aging	1 st Year			3
		Every Year After 1 st			1	ppm

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Measurement taken with outputs terminated with 50 ohm to $V_{DD}-2 \text{ V}$. See Figure 5.

4. Parameter guarantees 10 years of aging. Includes initial stability at 25°C , shock, vibration, and first year aging.

* Please contact sales office for availability

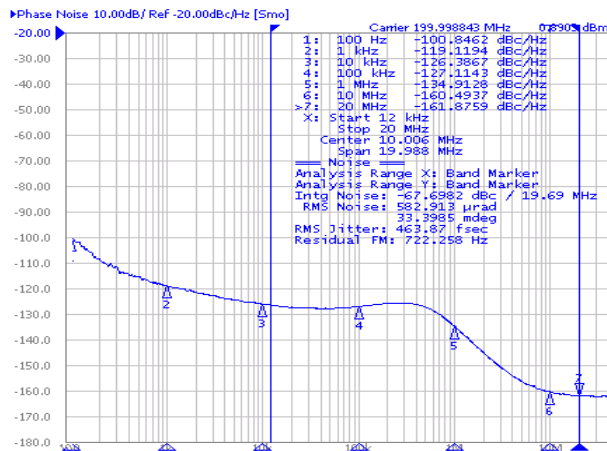


Figure 3. Typical Phase Noise Plot @ 200 MHz

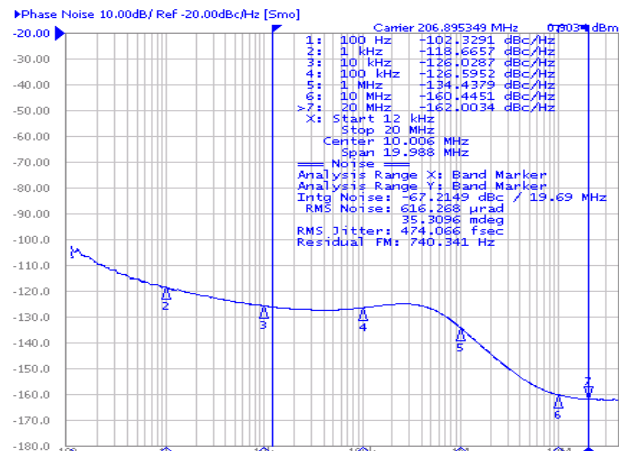


Figure 4. Typical Phase Noise Plot @ 206.9 MHz

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Table 8. RELIABILITY COMPLIANCE

Parameter	Standard	Method
Shock	Mechanical	MIL-STD-833, Method 2002, Condition B
Solderability	Mechanical	MIL-STD-833, Method 2003
Vibration	Mechanical	MIL-STD-833, Method 2007, Condition A
Solvent Resistance	Mechanical	MIL-STD-202, Method 215
Thermal Shock	Environment	MIL-STD-833, Method 1011, Condition A
Moisture Level Sensitivity	Environment	MSL1 260°C per IPC/JEDEC J-STD-020D

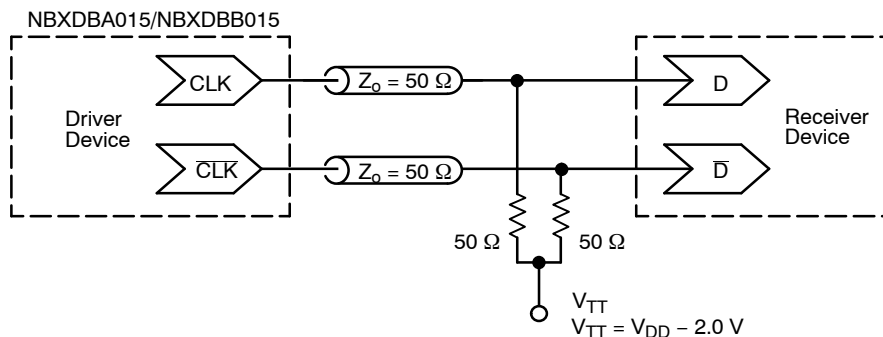


Figure 5. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

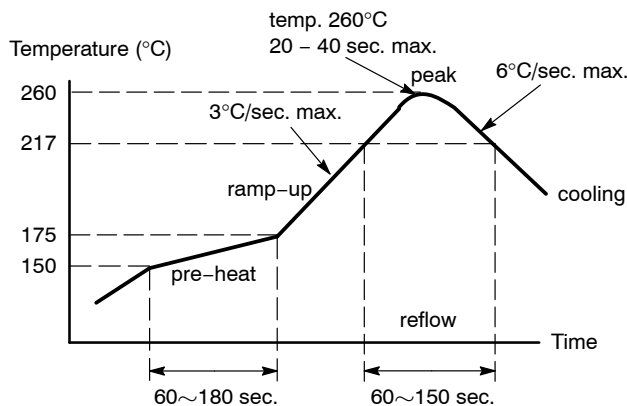
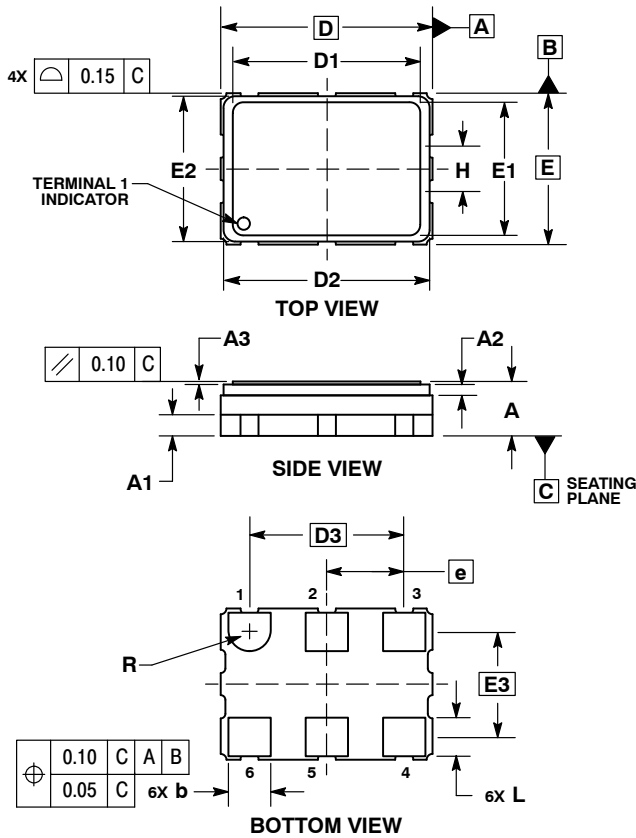


Figure 6. Recommended Reflow Soldering Profile

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PACKAGE DIMENSIONS

6 PIN CLCC, 7x5, 2.54P
CASE 848AB-01
ISSUE C

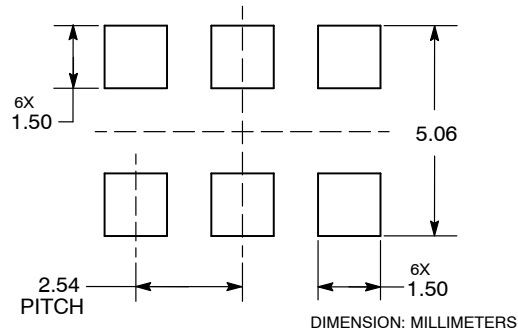


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	1.70	1.80	1.90
A1	0.70 REF		
A2	0.36 REF		
A3	0.08	0.10	0.12
b	1.30	1.40	1.50
D	7.00 BSC		
D1	6.17	6.20	6.23
D2	6.66	6.81	6.96
D3	5.08 BSC		
E	5.00 BSC		
E1	4.37	4.40	4.43
E2	4.65	4.80	4.95
E3	3.49 BSC		
e	2.54 BSC		
L	1.17	1.27	1.37
R	0.70 REF		

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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